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- Technology, Media & Telecom:
Semiconductor Capital Equipment
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Key Takeaways from 2014 SPIE and Meeting w/ ASML Management

The Cowen Insight

We met with ASML mgmt and toured both the EUV and immersion tool manufacturing facility in Veldhoven, Netherlands. Overall, ASML continues to operate to a financial model that implies ~€9B revs and ~€7/share of “peak” EPS in the 2017/2018 timeframe. More near term, ASML's order book should support a strong CQ3 but CQ4 is questionable as 2H:14 16/14nm ramp at Samsung/GF remains at risk.

Update from Meeting w/ ASML Management in Veldhoven, Netherlands

We met with ASML(€61.14, Outperform, €80 PT) management and toured both the EUV and immersion tool manufacturing facility in Veldhoven, Netherlands. Overall, ASML continues to operate to a financial model that implies ~€9B revs and ~€7/share of “peak” EPS in the 2017/2018 timeframe. This revenue model assumes ~€5B EUV (50 systems @ €100MM), €1.5B service, €1.5B legacy litho tools (a combination of primarily immersion and KrF for non-critical layers), and €1B holistic litho (a combination of hardware/software).

More near-term, the company is overall suggesting that EUV ramp issues (at least to the 80wph level) have shifted from “science” to “industrialization”, in other words, it is now a question of time given logistics and learning curve as the new MOPA upgrades are rolled out to the field for existing tools and those that have yet to ship. With respect to follow-on orders, the company continues to suggest TSMC only requires ~100 wafers/day throughput to commit to follow-on 3350NXE orders in 2H:14 for 10nm development. Given the current tool throughput that should be in the ~15wph range with stable dose control following the field upgrade (and uptime that ASML says has improved to ~80% - albeit in its own factory) uptime improvements are fairly pedestrian to start to finally secure a next batch of orders later this year. A more meaningful achievement remains 500 wafers/day which is achievable with ~60-70 wph throughput running at ~70% uptime); this remains a ways away pending a broader rollout of reliability, power and performance upgrades.

From a business perspective, in addition to its standing 1H:14 guidance, our work still indicates ASML's order book should also support a strong CQ3 but CQ4 does remain somewhat of a question as TSMC has already taken delivery of ~50k wsm of 20nm capacity in 2H:13, 14nm ramp at INTC(\$24.76, Market Perform, \$23.50 PT) continues to slide a little bit, and Samsung and GF do not appear all that close to locking down 16/14nm processes sufficiently to place litho orders before 2H:14 for shipment in 1H:15.

Key Takeaways From 2014 SPIE Lithography Conference

This week we attended SPIE Advanced Lithography 2014 in San Jose, CA - the largest tradeshow for lithography related to the semiconductor industry. The main updates were incremental improvement to source data from Cymer/ASML, EUV progress updates from customer (TSMC, Intel) and a lot of updates on alternative lithography. Please see addendum of this report for important disclosures.

techniques (DSA, Self aligned multi patterning, e-beam, Nano imprint). While TSMC/ Intel reiterated their existing EUV insertion timeline of late 10nm/7nm respectively, our work suggests that TSMC will mostly likely insert in 7nm (~2019). With respect to INTC, its tone on EUV has changed slightly as the door sounds more open for EUV insertion at 7nm (2019) relative to prior suggestion that it didn't really need EUV until 5nm. More importantly, 7nm design rules are expected to include more self-aligned patterning (vs. current lithography intensive double patterning process), with more etch/dep steps than litho steps, a positive for AMAT(\$18.96, Outperform, \$20 PT)/ LRCX(\$51.73, Outperform,\$58 PT).

From fabless customer perspective, Qualcomm highlighted the increasing patterning challenges associated with sub 28nm designs and noted the design complexity has increased the cost/wafer significantly (20/14nm – 2.5x 65nm and 10nm – 1.4x 20nm). The company highlighted that cost is the most important factor that drives design optimization as \$ value of SoC is relatively fixed (Average SoC ASP ~\$30 w/ advanced chips <\$50). More importantly, Qualcomm noted that the new technology product design will be ready ~1 year after manufacturing process is ready, which in our view implies that Qualcomm will most likely ramp 16/14nm products in 2H:15/1H:16 as 16/14nm technology development is still ongoing at TSMC/Samsung.

EUV source update

Compared to SPIE 2013, ASML's progress in source power (30W in production mode @ customer site and demonstrating 70wph (source: 105W) capability by YE2014) is ~6 months delayed but the company, in our view, has made some progress on source power and overall EUV system CoO. The NXE3300 MOPA PP field upgrade in CQ1:14 is expected to increase the source power from 10W to 30W (~15wph from 8wph previously), just enough for customers (TSMC/Intel) to start 10nm/7nm technology development work. Relative to a year ago, ASML is also more confident of implementing 80W/55wph in production in 2014, largely driven by the use of new dose control system and improved system efficiency (CE>5%). More importantly, in-situ Hydrogen cleaning of collectors looked promising w/ a potential to reduce cost of ownership significantly (higher tool availability – 40-60%) by extending collector tool life (> 6 months) but field upgrades may not happen until 2H:14 as customers remain focused on technology development over CoO improvements now. While the introduction of EUV in HVM largely depends on relative cost per wafer (EUV vs. alternatives), ASML still remains confident that EUV would be used for 1-2 layers (in our view – BEOL Mx layers) at 10nm (late insertion – ~2018 in our view) by TSMC/ Samsung and full production ramp at 7nm (~2019, in our view) by TSMC/Samsung/ Intel.

Alternative Lithography Updates

While many alternative techniques were presented, in our view, DSA (Directed Self Assembly) and Self-aligned multiple patterning (SADP/SAQP) looked more promising from a year ago. DSA ecosystem has made significant progress, especially on defects (down by a factor of 100) but our work suggests that DSA is not expected to replace EUV but rather remain a complementary technology w/ applications limited to contact holes at 10nm and potentially L/S at 7nm. Self-aligned multiple patterning is viewed as a potential replacement of EUV in certain critical layers (M1) especially if EUV throughput is less than 85 wph. On e-beam, while the technology looks promising especially for contact hole applications, in our view, there has not been much progress made on this front compared to last SPIE. Relative to Nano imprint technology,

Molecular Imprint (now part of Canon) noted that its technology will be used in advanced memory technologies (15nm Planar NAND) by Toshiba in 2015 (see our note [Assessing Impact from Canon Buying Molecular Imprints](#) published 2/13/2014). However, we continue to believe that Nano imprint technology is not mature enough to replace immersion or EUV in the near future, especially in foundry/logic markets, as company data suggests that 2015 throughput could at best reach ~10-20wph (vs. immersion throughput ~250 wph) and defects/cm² still much higher than existing non-contact lithography processes.

Competitive dynamics in immersion (193i) lithography

Nikon presented their immersion update on Sunday in a separate company event (Nikon Vision). Nikon will introduce 630D into market in 2014 with improved throughput (250wph) vs. 622D of >200 wph and overlay capability (single tool -1.7nm) vs. 622D of <2nm. Interestingly, Nikon didn't update the MMO overlay capability (immersion tool to EUV tool), which in our view could imply that Nikon immersion tool would mostly likely be used standalone only (only at Intel, in our view). On 450mm, while ASML has effectively stopped investing in 450mm tool (per Intel's request based on company filings), Nikon is continuing to develop 450mm tools and expected to ship first tools to G450C in 2015. While the delay in EUV adoption has given Nikon some breathing room, we continue to remain skeptical on Nikon gaining litho share at TSMC/Samsung given a) Nikon's history of overpromising on performance but under delivering and b) more importantly, the high barriers to entry created by ASML's holistic litho features.

Valuation Methodology And Risks

Valuation Methodology

Semiconductor Capital Equipment:

Our valuation methodology is primarily based on forward P/E multiples plus cash followed by EV/EBITDA. In many cases, we use EV/sales as a third methodology.

Semiconductors:

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Semiconductors:

The semiconductor industry is cyclical and has strong correlation to global GDP. If global growth slows, consumer demand and IT spending could impact our forecasts. Additionally, pricing pressure is severe in certain parts of the market, particular those that are consumer focused.

Addendum

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ASML.NA	ASML Holding NV
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LRCX	Lam Research

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Assumption: The expected total return calculation includes anticipated dividend yield

Cowen and Company Rating System until May 25, 2013

Outperform (1): Stock expected to outperform the S&P 500

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Assumptions: Time horizon is 12 months; S&P 500 is flat over forecast period

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Cowen And Company Rating Definitions

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Rating	Count	Ratings Distribution	Count	IB Services/Past 12 Months
Buy (a)	415	59.20%	68	16.39%
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Sell (c)	16	2.28%	1	6.25%

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Legend for Price Chart:

I = Initiation | 1 = Outperform | 2 = Market Perform | 3 = Underperform | UR = Price Target Under Review | T = Terminated Coverage | \$xx = Price Target | NA = Not Available

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